ABSTRACT

A system for instruction memory storage and processing in a computing device
having a processor, the system is based on backwards branch control information and
comprises a dynamic loop buffer (DLB) which is a tagless array of data organized as a

5   direct-mapped structure; a DLB controller having a primary memory unit partitioned into
a plurality of banks for controlling the state of the instruction memory system and
accepting a program counter address as an input, the DLB controller outputs distinct
signals. The system further comprises an address register located in the memory of the
computing device, it is a staging register for the program counter address and an

10   instruction fetch process that takes two cycles of the processor clock; and a bank select
unit for serving as a program counter address decoder to accept the program counter
address and to output a bank enable signal for selecting a bank in a primary memory unit,
and a decoded address for access within the selected bank.